What is claimed is:

1. A packet processing unit for outputting a packet to a transmission channel after performing destination address on said packet received from said transmission channel, comprising:

packet receiving means for outputting the packet received via said transmission channel in the form of split cells of a fixed length,

search key extracting means for extracting a predetermined search key from said cells received from said packet receiving means,

CAM for performing retrieval based on said search key extracted in said search key extracting means and outputting memory address corresponding to said key

associative data storing means for storing at least destination information and for outputting the information stored in the input memory address,

associative data reading means for calculating the memory address of said associative data storing means based on said memory address received from said CAM and supplying the memory address to said associative data storing means,

destination address means for performing destination address of a particular cell based on the information of said associative data storing means read by said associative data reading means, and

packet transmitting means for putting the cells received

from said destination address means back to a packet and outputting said packet to said transmission channel,

wherein said packet receiving means, search key extracting means, CAM, associative data storing means, associative data reading means, destination address means and packet transmitting means perform a pipeline processing.

2. A packet processing unit as claimed in claim 1, wherein duration of each stage of said packet receiving means, search key extracting means, CAM, associative data storing means, associative data reading means, destination address means and packet transmitting means are set at not more than arriving time interval of the packet input in said packet receiving means.

3. A packet processing unit as claimed in claim 2, wherein processing time of said packet receiving means, search key extracting means, CAM, associative data storing means, associative data reading means, destination address means and packet transmitting means are set at not more than the duration of each stage.

4. A packet processing unit as claimed in claim 3, comprising maintenance means for performing maintenance of at least one of said CAM or said associative data storing means during idle time of said stage.

5. A packet processing unit as claimed in at least one of claim

1 though 4, comprising buffer means for a timing adjustment between said transmission channel and said packet receiving means and between said transmission channel and said packet transmitting means.

6. A packet processing unit as claimed in at least one of claim 1 though 5, comprising arithmetic processing means for performing a predetermined process with respect to said cells in at least one of a following step to said packet receiving means or a preceding step to said packet transmitting means.